REMARKS/ARGUMENTS

The Office action issued 23 April 2003 indicates that claims 174 and 175 are pending in the application. It appears that a second preliminary amendment filed in this case on 7 November 2001 and received in the USPTO mailroom on 16 January 2002 did not find its way to the Examiner's desk. A copy of the Second Preliminary Amendment together with a copy of the postcard indicating its receipt by the USPTO mailroom is enclosed for the convenience of the Examiner.

The Second Preliminary Amendment amended claim 174 to remove the words "the steps of" after the word "comprising". That change was made because applicant did not intend to invoke 112 paragraph 6 (step plus function) and therefore removal of that language eliminates any possible ambiguity. No change in claim scope was intended. Claim 175 was also amended to replace Vt with Vth. No change in scope was intended.

In addition to amending claims 174 and 175, new claims 176 –181 were added.

In response to paragraph 1 of the Office action, the informalities in the specification identified by the Examiner have been corrected. The undersigned attorney is not responsible for the prosecution of the applications mentioned in the specification. Information regarding the current status of those applications has been requested of the assignee; the specification will be amended to reflect the updated status information as soon as such information is received.

In paragraph 2 of the Office action, claims 174 and 175 are rejected under 35 U.S.C. §112, first paragraph. The Examiner's attention is respectfully directed to the paragraph beginning at line 24, page 62 and continuing over to line 14, page 63. It is respectfully submitted that support for not only claims 174 and 175, but also claims 176-181 may be found in the aforementioned paragraph as well as FIG. 6C.

In paragraph 3 of the Office action, claims 174 and 175 stand rejected under 35 U.S.C. §102(b) as being anticipated by McAlexander. The Examiner has noted FIG. 3, and the accompanying discussion in column 4, lines 35-38 and also column 5, lines 3-7.

In response, claim 174 has been amended to make it clear that the rendering of the pair of transistors conductive occurs "during a write operation". Independent claim 177 has been similarly amended to add the language "during a write operation". Independent claim 179 is directed to a method "of enabling a write".

The section of McAlexander cited by the examiner (column 4, lines 35 – 38) is directed to a read operation. As stated in McAlexander at column, lines 35-39:

> This causes an imbalance in the voltage on the nodes 54 and 55, and the same differential is coupled to the nodes 52 and 53 because the voltage Ptr is higher than Vdd. The nodes will separate no more than perhaps fifty milivolts at this point. Then, when Psb1 goes high and the small transistor 62 turns on, *the sensing operation is initiated* and the nodes separate more as the bistable circuit including the transistors 50 and 51 goes toward a stable condition with one transistor conducting and the other cut off. [emphasis added]

A write operation in McAlexander is handled differently as discussed at the bottom of column 4, beginning at line 65.

> According to the invention, an active pull-up circuit is employed to allow storage of a full Vdd level. This circuit comprises a pair of pull-up transistors 66 and 67 connecting the nodes 54 and 55 to Vdd, along with control transistors 68 and 69 connecting the gates of the transistors 66 and 67 to the nodes 54 and 55, and capacitors 70 and 71 connecting the gates to a boosting clock Pb occurring after Psb2. *The gates of the transistors 68 and 69 are connected to a trap voltage Vtr which stays at a level of about 1 Vt below Vdd during the active part of the cycle then at Vdd during the precharge part.* The details of operation of the active pull-up circuit will be described below. [emphasis added]

Writing of a full Vdd is accomplished by raising the voltage level on the selected X line, not by driving a logic "one" through an isolation transistor.

> Then, about four ns. after Psb2 goes high, the selected X line is slowly boosted to a level of Vdd+Vt to permit restoration of a full Vdd level in the capacitor 40 for the selected cell. (column 5, lines 15-18)

It is respectfully submitted, based on the foregoing, that McAlexander neither anticipates nor renders obvious claims 174-181.

Finally, it is noted that certain of the claims have been amended to remove the language "step of" to insure that there is no ambiguity over whether applicant intended to invoke section 112, paragraph 6.

Please note that in the Second Preliminary Amendment (copy enclosed) there is a statement requesting deletion of inventor. More specifically, as a result of the manner in which this application has been prosecuted, Scott J. Derner is no longer an inventor. Please allow the instant application to proceed in the names of the remaining inventors, Keeth and Bunker.

Applicants have made a diligent effort to place the instant application in condition for allowance. Accordingly, a notice of allowance for claims 174-181 is respectfully requested. If the Examiner is of the opinion that the instant application is in condition for disposition other than through allowance, he is respectfully requested to contact applicants' attorney at the telephone number listed below so that additional changes may be discussed.

Respectfully submitted

Edward L. Pencoske
Reg. No. 29,688
Thorp Reed & Armstrong, LLP
One Oxford Centre
301 Grant Street, 14th Floor
Pittsburgh, PA 15219-1425
(412) 394-7789

Attorneys for Applicants

I hereby certify that this correspondence is being deposited in the United States Postal Services as First Class Mail in an envelope address to:

Commissioner for Patents
Washington, D.C. 20231

Attorney for Applicants

Date: 7 Nov. 2001

COPY

PATENT
Attorney Docket No.: DB000575-023

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Keeth, et al.	)	
		)	**Examiner:** Not yet assigned
Serial No.:	09/934,795	)	
		)	**Art Unit:** 2816
Filed:	22 August 2001	)	

Entitled: 256 MEG DYNAMIC RANDOM ACCESS MEMORY

~~SECOND PRELIMINARY AMENDMENT~~

Preliminary to the examination of the above-identified application, please amend that application as follows.

In the claims

Please amend claims 174 and 175 as follows.

174. (Amended) A method of controlling the conduction of a pair of isolation transistors in a sense amplifier responsive to an array, comprising [the steps of]:

rendering the pair of transistors conductive with a control signal that is a boosted version of the voltage used by the array; and

rendering the pair of transistors nonconductive by removing said control signal.

175. (Amended) The method of claim 174 wherein said step of rendering the pair of transistors conductive includes the step of rendering the transistors conductive with a control signal that is approximately a [Vt] Vth higher than the voltage used by the array.

Please add the following new claims.

176. The method of claim 174 wherein said step of rendering the transistors conductive includes the step of rendering the transistors conductive with a control signal that enables the full voltage representative of a logic level one to be written to the array.

177. A method of controlling the conduction of at least one isolation transistor in a sense amplifier responsive to an array, comprising:

rendering the transistor conductive with a control signal that enables a full Vcc to be conducted by the isolation transistor; and

rendering the transistor nonconductive by removing said control signal.

178. The method of claim 177 wherein said step of rendering the transistor conductive includes the step of rendering the transistor conductive with a control signal that is approximately a Vth higher than Vcc.

179. A method of enabling a write to a memory array of the full voltage representative of a logic level one using a sense amplifier in which the sense amplifiers are located inside the isolation transistors, comprising:

rendering the isolation transistors conductive with a control signal that compensates for the voltage drop across the isolation transistors.

180. The method of claim 179 wherein said rendering step includes the step of rendering the isolation transistors conductive with a control signal that is approximately a Vth higher than the voltage used to represent a logic level one.

181. The method of claim 180 wherein said control signal is approximately Vth plus Vcc.

REMARKS

New claims 176 – 181 are presented for examination. The claims are supported by, for example, FIG. 6C and the text in the paragraph bridging pages 62 and 63. No new matter has been entered.

STATEMENT REQUESTING DELETION OF INVENTOR

As a result of the prosecution of this application, the following individual is no longer an inventor of the subject matter being claimed and should be removed as an inventor:

Scot J. Derner

Please allow the instant application to proceed in the names of the remaining inventors (Keeth and Bunker) in accordance with 37 CFR 1.63 (d).

It is respectfully requested that the instant application, covering claims 174 – 181 receive an early office action on the merits.

Respectfully submitted

Edward L. Pencoske
Reg. No. 29,688
Thorp Reed & Armstrong, LLP
One Oxford Centre
301 Grant Street, 14th Floor
Pittsburgh, PA 15219-1425
(412) 394-7789
Attorneys for Applicants

Dated: 7 November 2001

PATENT
Attorney Docket No.: DB000575-023

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Keeth, et al.	)	
		)	Examiner: Not yet assigned
Serial No.:	09/934,795	)	
		)	Art Unit: 2816
Filed:	22 August 2001	)	

Entitled: 256 MEG DYNAMIC RANDOM ACCESS MEMORY

COMPLETE CLEAN SET OF PENDING CLAIMS

174. (Amended) A method of controlling the conduction of a pair of isolation transistors in a sense amplifier responsive to an array, comprising:

rendering the pair of transistors conductive with a control signal that is a boosted version of the voltage used by the array; and

rendering the pair of transistors nonconductive by removing said control signal.

175. (Amended) The method of claim 174 wherein said step of rendering the pair of transistors conductive includes the step of rendering the transistors conductive with a control signal that is approximately a Vth higher than the voltage used by the array.

176. The method of claim 174 wherein said step of rendering the transistors conductive includes the step of rendering the transistors conductive with a control signal that enables the full voltage representative of a logic level one to be written to the array.

177. A method of controlling the conduction of at least one isolation transistor in a sense amplifier responsive to an array, comprising:

rendering the transistor conductive with a control signal that enables a full Vcc to be conducted by the isolation transistor; and

rendering the transistor nonconductive by removing said control signal.

178. The method of claim 177 wherein said step of rendering the transistor conductive includes the step of rendering the transistor conductive with a control signal that is approximately a Vth higher than Vcc.

179. A method of enabling a write to a memory array of the full voltage representative of a logic level one using a sense amplifier in which the sense amplifiers are located inside the isolation transistors, comprising:

rendering the isolation transistors conductive with a control signal that compensates for the voltage drop across the isolation transistors.

180. The method of claim 179 wherein said rendering step includes the step of rendering the isolation transistors conductive with a control signal that is approximately a Vth higher than the voltage used to represent a logic level one.

181. The method of claim 180 wherein said control signal is approximately Vth plus Vcc.

The dating stamp of the USPTO on this card will be taken as an indication that the accompanying paper(s) was filed.

Applicant(s) Keeth, et al.
Serial No. 09/934,795
Filing Date 22 August 2001
Amount of Check N/A
Atty's File No. DB000575-023
ELP/mep
7 November 2001

*Transmittal Letter
*Second Preliminary Amendment with Complete Clean Set of Pending Claims Attached

The dating stamp of the USPTO on this card will be taken as an indication that the accompanying paper(s) was filed.

Applicant(s) Keeth, et al.
Serial No. 09/934,795
Filing Date 22 August 2001
Amount of Check N/A
Atty's File No. DB000575-023
ELP/mep
7 November 2001

*Transmittal Letter
*Second Preliminary Amendment with Complete Clean Set of Pending Claims Attached